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Respectfully Submitted,

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(54) NONVOLATILE MEMORY AND ELECTRONIC APPARATUS

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(73) Assignee: Semiconductor Energy Laboratory Co., Ltd. (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

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See application file for complete search history.

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(57) ABSTRACT

An active region, a source region, and a drain region are formed on a single crystal semiconductor substrate or a single crystal semiconductor thin film. Impurity regions called pinning regions are formed in striped form in the active region so as to reach both of the source region and the drain region. Regions interposed between the pinning regions serve as channel forming regions. A tunnel oxide film, a floating gate, a control gate, etc. are formed on the above structure. The impurity regions prevent a depletion layer from expanding from the source region toward the drain region.

45 Claims, 17 Drawing Sheets